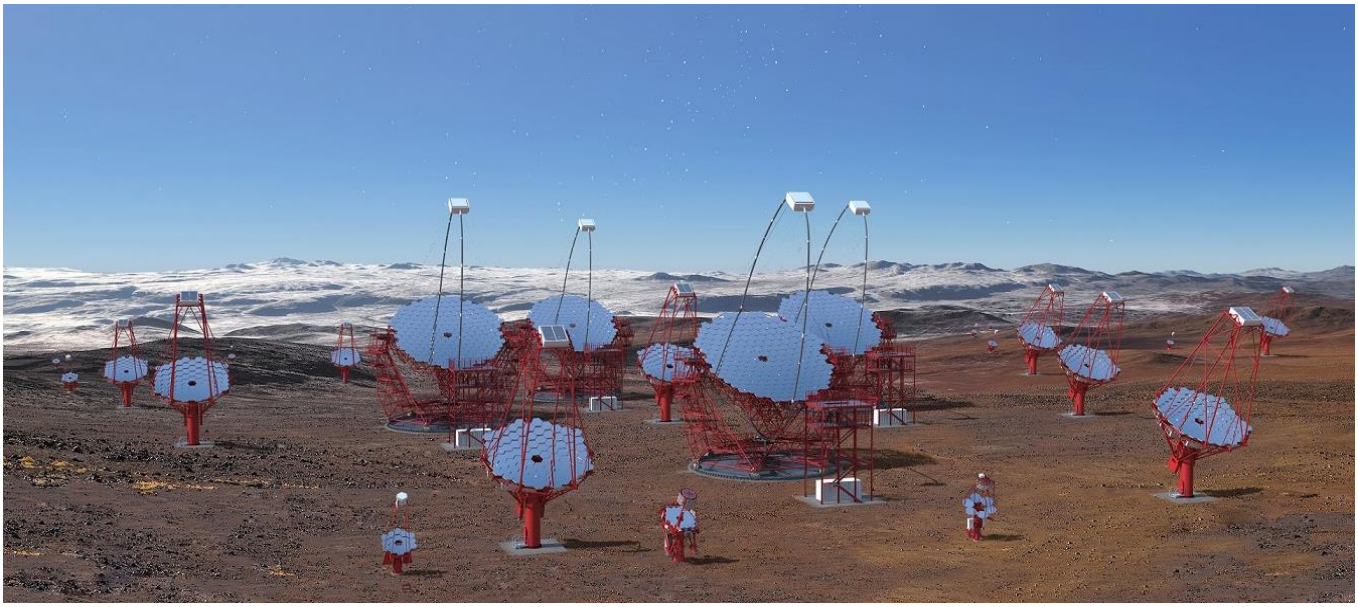
Influence of the continuous light flux on the SiPM gain by using Weeroc QFP and BGA packages CITIROC 1A evaluation boards



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LIST OF ACRONYMS

OACT	Osservatorio Astrofisico di Catania
IFC	Istituto di Astrofisica Spaziale e Fisica Cosmica di Palermo
COLD	Catania astrophysical Observatory Laboratory for Detectors
PCB	Printed Circuit Board
SiPM	Silicon Photo-Multiplier
MPPC	Multi Pixel Photon Counter
SST-2M	Small-Size Telescope Dual-Mirror
PDM	Photon Detection Module
ASIC	Application Specific Integrated Circuit
FEE	Front-End Electronics
BEE	Back-End Electronics
FPGA	Field Programmable Gate Array
EASIROC	Extended Analogue Silicon-pm Integrated Read-Out Chip
CITIROC	Cherenkov Imaging Telescope Integrated Read-Out Chip
I/F	Interface
LCT	Low Cross Talk
PSAU	Power Supply and Amplification Unit
PDE	Photon Detection Efficiency
SCA	Switched Capacitor Array
OCT	Optical Cross Talk
LVR	Low Voltage Resistor
LVR2	Low Voltage Resistor 2nd Version
LVR3	Low Voltage Resistor 3nd Version
PHD	Pulse Height Distribution

1. INTRODUCTION

The scope of this work is to evaluate the influence of the of the continuous light flux generated by an LED on the SiPM gain by using Weeroc QFP and BGA packages CITIROC 1A evaluation boards. This document illustrates the experimental setup developed to measure the gain degradation on a single 7x7 mm^2 SiPM illuminated with a pulsed LED, due to the increasing illumination on an array of 2x2 7x7 mm^2 SiPM array and the obtained results. Relevant parameters configuration adopted in the CITIROC User Interface (V0.9.8129) for the measurements is also reported.

We used two different light-tight boxes: one for the single pixel and one for the array, in such a way to illuminate only the array with the continuous source.

The test is essentially based in staircase measurements of the single pixel illuminated by a pulsed LED while illuminating the SiPM array with an LED powered by a DC power supply whose level is varied in order to change the current flowing in the HV circuit.

Not changing the SiPMs operating voltage (Vop) and increasing the intensity of the continuous source, we found an increasing in the HV circuit current and a decreasing of the SiPM gain.

As the gain depends on the Vop, to obtain the same initial SiPM gain, we increased the Vop by setting the anode voltage level through the DAC input.

For these measurements five 7x7 mm^2 LVR3 MPPC-7075 non coated have been used.

The achieved results in the various operating conditions are here presented.

2. Experimental Setup

The adopted experimental setup is shown in Figure 1. As can be seen, two different light-tight boxes have been used: one small for the single pixel and one large for the 2x2 pixel array. In this way, the apparatus allows to illuminate separately the array with the continuous source and the single pixel with the pulsed LED source.

Through an electronic adapter we are able to mount the light-tight boxes system in both QFP and BGA CITIROC 1A evaluation boards.

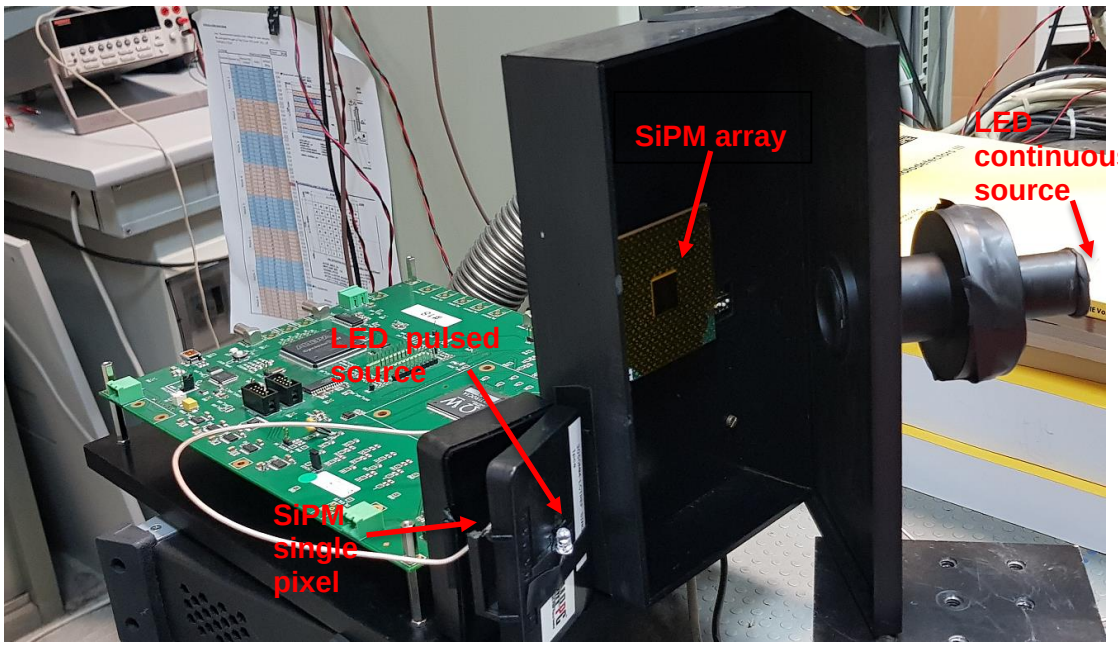


Figure 1. Experimental setup based on the use of pulsed light source that illuminates a single 7x7 mm^2 SiPM and a continuous light source that illuminates a 2x2 7x7 mm^2 pixel array

The system is constituted by:

- Power supply Agilent 6634B
  (to supply the high voltage to the SiPM)
- Power supply Agilent E3631A
  (to supply the voltage levels to the pulsed LED and to continuous LED source)
- Multimeter Keithley 2000
  (to measure the current flowing in the HV circuit)
- Oscilloscope LeCroy wavePro 725Zi 2.5GHz
  (to process synchro signals for the pulsed light source)
- Pulse generator LeCroy ArbStudio 1104
  (to generate synchro signals for the pulsed light source)

3. Staircase measurements in different operating conditions

We carried out the staircase measurements through both BGA and QFP CITIROC 1A evaluation boards.

3.1 QFP CITIROC 1A staircase measurements

The measurements have been done by using the new software "Citiroc User Interface (V0.9.8129)". The main settings are shown in Figure 2, We selected:

- ✓ Use peak sensing (high gain)
- ✓ High gain to fast shaper
- ✓ shaping time 25 ns

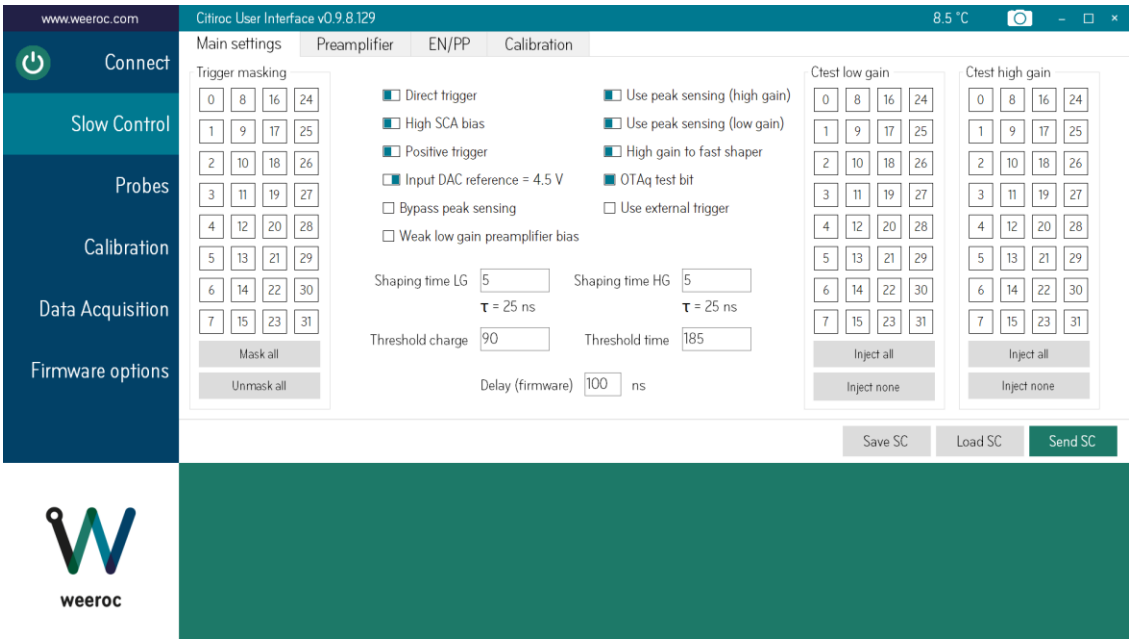


Figure 2. Screenshot of the main settings: Peak detector, high gain to fast shaper and shaping time 25 ns have been selected.

The preamplifier settings are shown in Figure 3, the selected channels are ch0 for the single pixel, ch1, ch7, ch25 and ch31 for the four pixel mounted in the tile. The high gain is settled to 66.6 (corresponding to 54) and the low gain is settled to 3.33 (corresponding to 45). All the other channels are disabled.

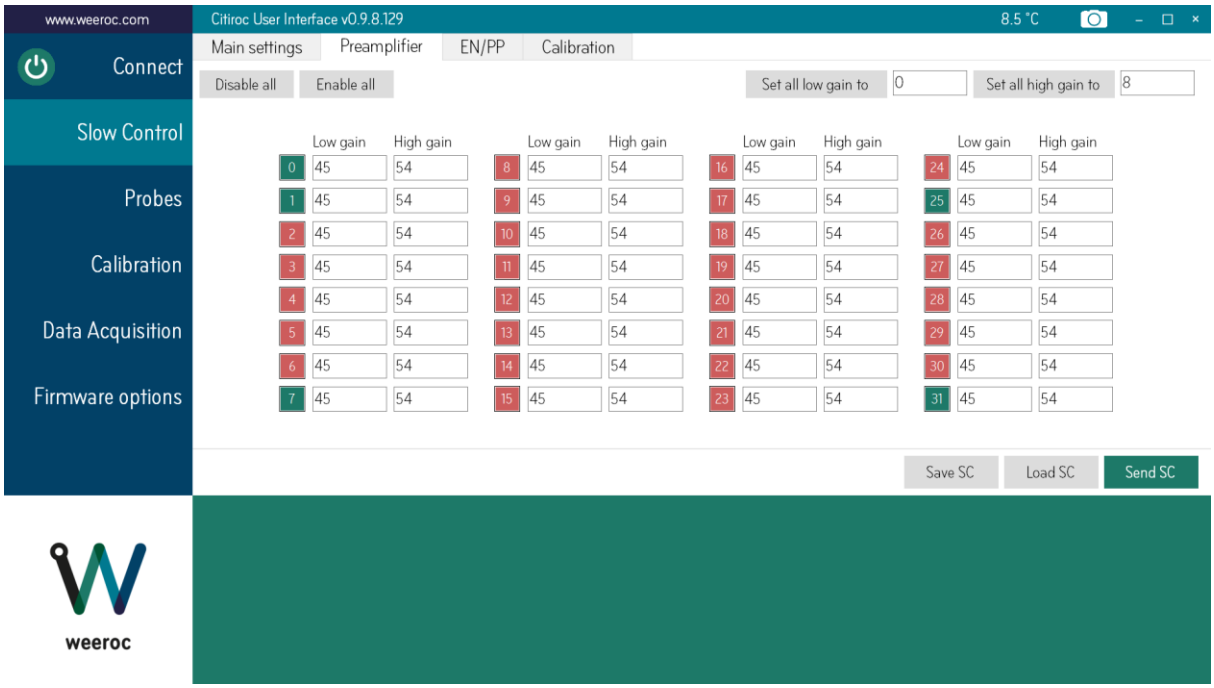


Figure 3. Screenshot of the preamplifier settings: the selected channels are ch0 for the single pixel, ch1, ch7, ch25 and ch31 for the four pixels mounted in the tile. The high gain is settled to 66.6 (corresponding to 54) and the low gain is settled to 3.33 (corresponding to 45). All the other channels are disabled.

The CITIROC 1A package QFP has been test in two ways: one with the input DAC set to about 2.4 V that means set to 128 (see figure 4):

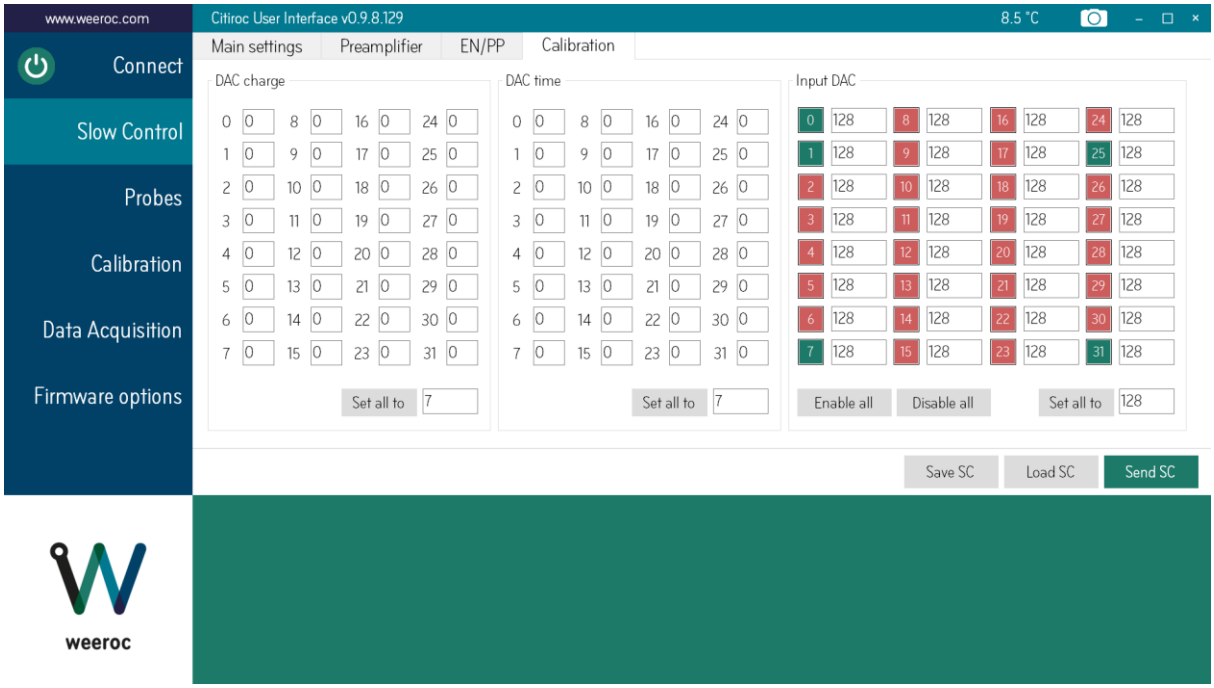


Figure 4. Screenshot of the input DAC settings: The input DAC of all channels are set to 128, meaning that we set the channel to about 2.4 Volt.

Operating the MPPCs with the above mentioned conditions we carried out the staircase measurements. Figure 5 shows the staircases obtained at different current flowing in the HV circuit produced by illuminating the 2x2 7x7 mm^2 with the continuous source.

The black line is the reference one, obtained by operating the SiPM at 3V of Over-Voltage. As can be noted at a current of 100µA no relevant distortion is observed, while from 0.5 mA to 1.6 mA a gain degradation and an unexpected drop of the plot at higher DAC valued is also observed.

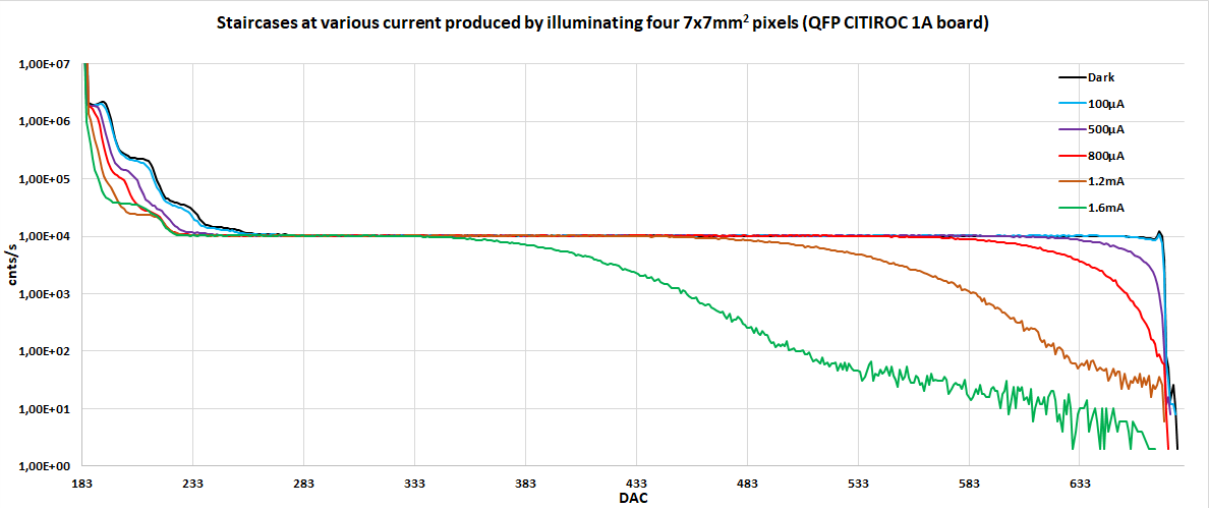


Figure 5. Staircases obtained at different current flowing in the HV circuit produced by illuminating the 2x2 7x7 mm^2 with the continuous source. From 0.5 mA to 1.6 mA a gain degradation and an unexpected drop of the plot at higher DAC is also observed.

To better estimate the gain degradation we reported in figure 6 the first part of the staircases.

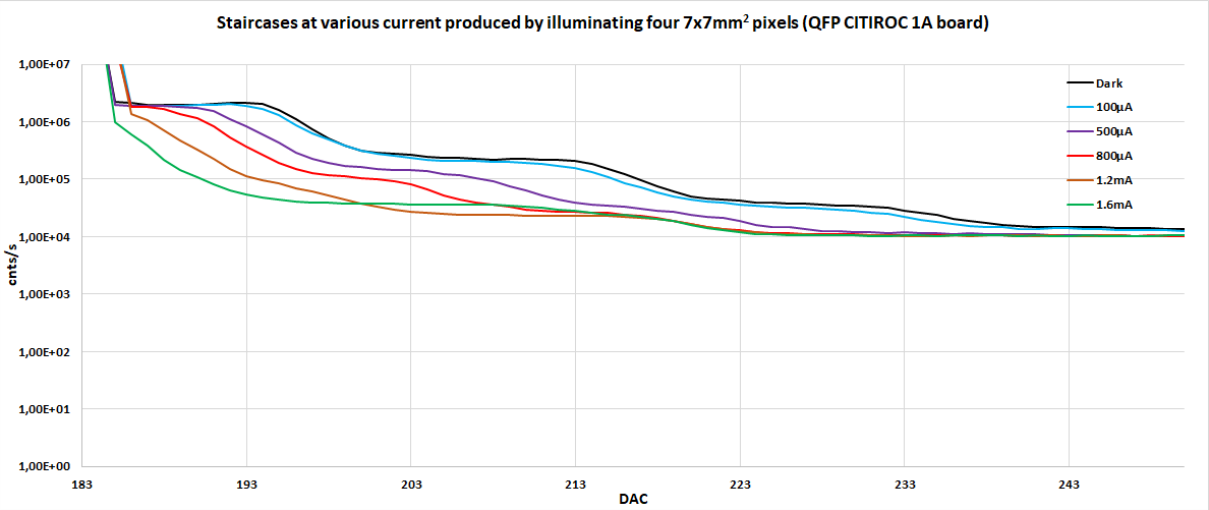


Figure 6. Details of the staircases of the figure 5.

As the gain depends on the Vop, to obtain the same initial SiPM gain, we increased the Vop at higher values by setting the anode voltage level through the DAC input The results are shown in figure 7. The figure report the staircases obtained at different current flowing in the HV compensated by setting the anode voltage level through the DAC input. By setting the DAC input at the appropriate level, the green dotted plot (1.2 mA), the violet dotted plot (1.5 mA) and the red dotted (1.8 mA) result perfectly recovered at the initial gain and the unexpected drop at the end of the DAC disappeared.

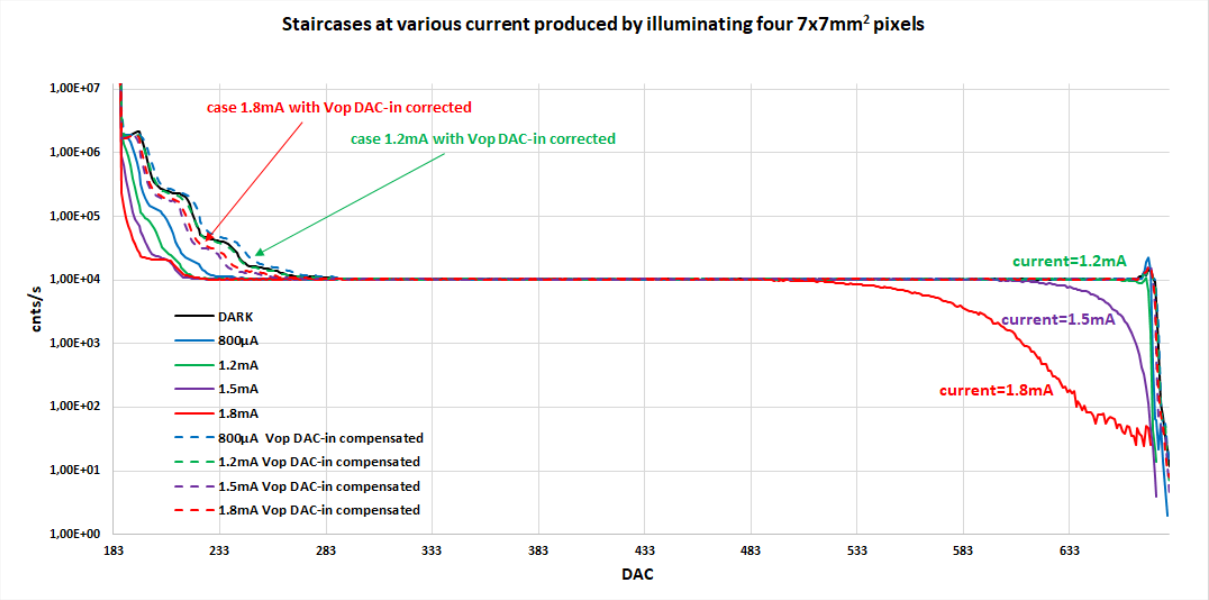


Figure 7. Staircases obtained at different current flowing in the HV compensated by setting the anode voltage level through the DAC input. By setting the DAC input at the appropriate level, the green dotted plot (1.2 mA), the violet dotted plot (1.5 mA) and the red dotted (1.8 mA) result perfectly recovered at the initial gain and the unexpected drop at the end of the DAC disappeared.

To better estimate the gain recovering we reported in figure 8 the first part of the staircases.

As can be noted the dotted plots shows how the gain degradation is completely recovered by increasing the DAC input voltage level.

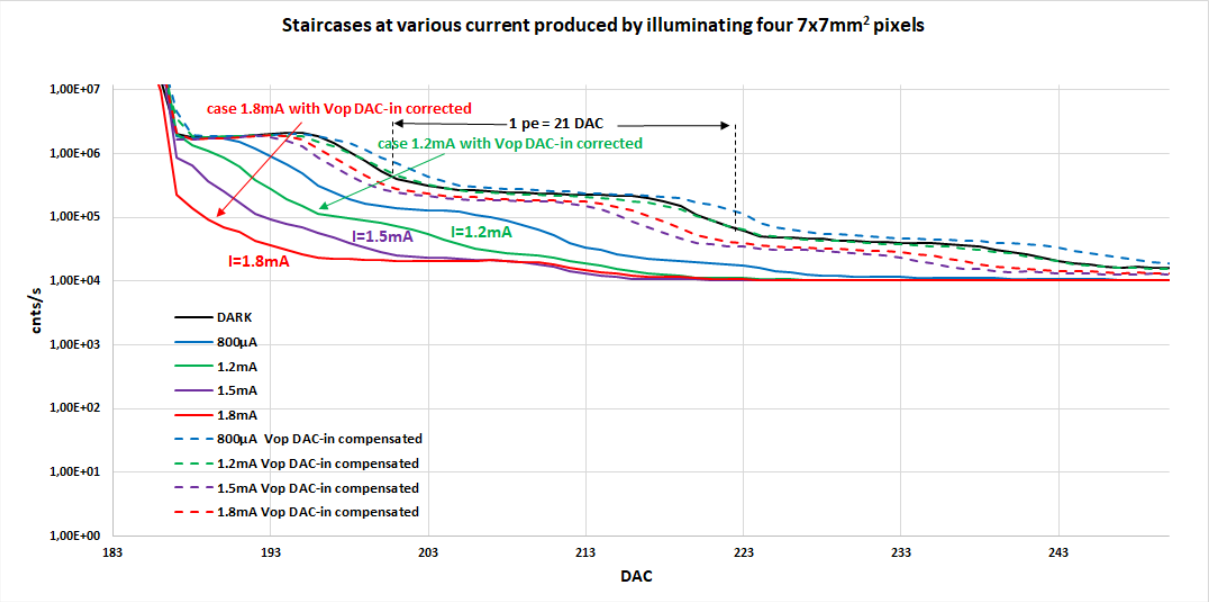


Figure 8. First part of the staircases of the figure 5. As can be noted the dotted plots shows how the gain degradation is completely recovered by increasing the DAC input voltage level.

The effect of Vop decreasing is to be attributed to the 1KOhm resistor in the HV circuit. Then we shortened the resistor and repeated the staircase measurements.

In Figure 9 is shown the staircases obtained at 2.2 mA current flowing in the HV circuit. As can be seen no effect are present both in gain variation and drop in the final part of the plot.

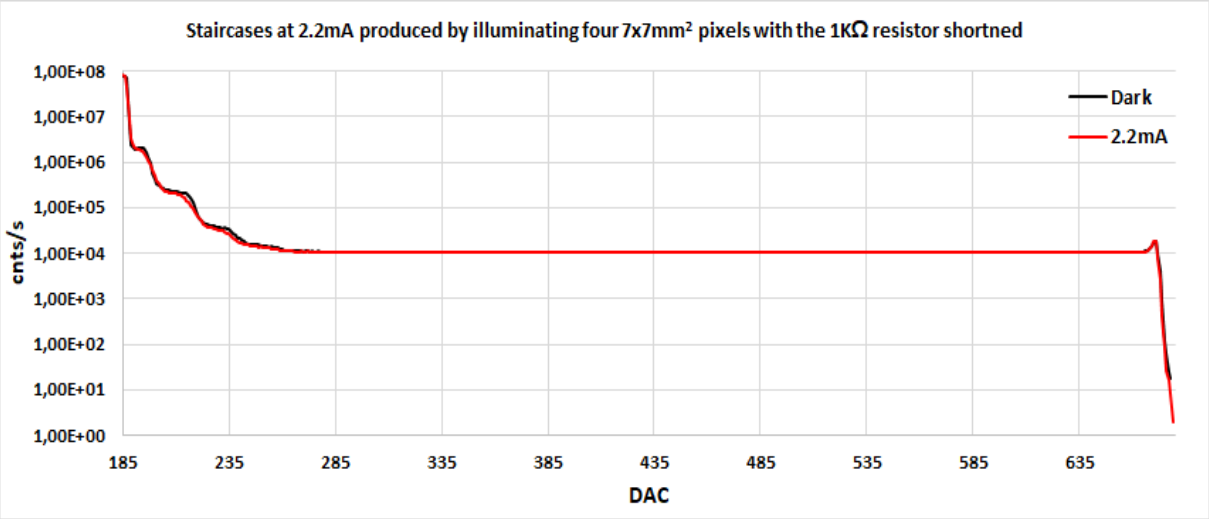


Figure 9. Staircases obtained in dark condition and with 2mA current flowing in the HV circuit. As can be seen no effect are present both in gain variation and drop in the final part of the plot.

In figure 10 the first part of the staircases shows that no gain degradation happens.

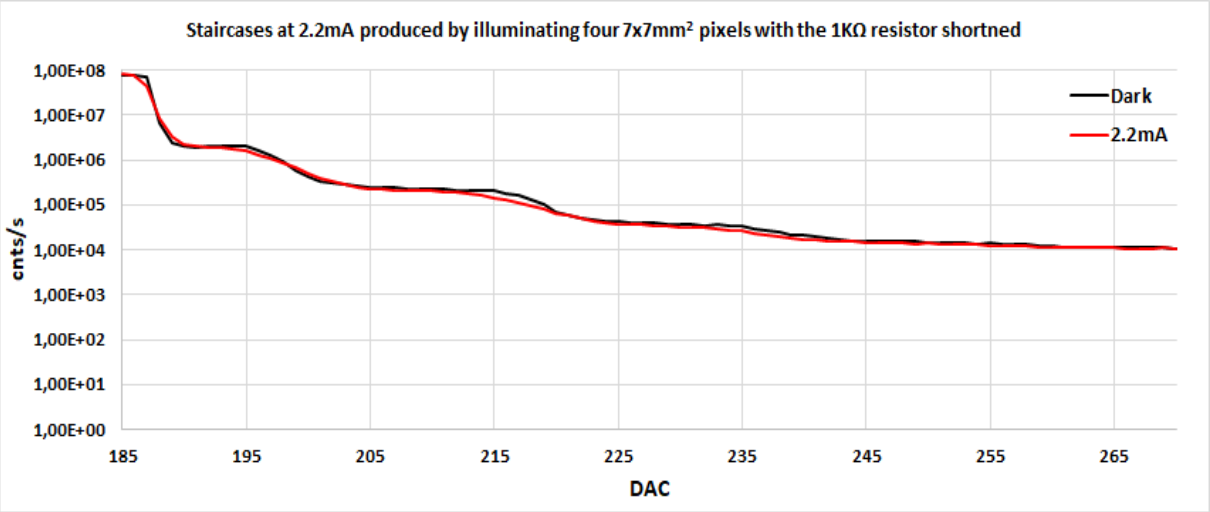


Figure 10. First part of the staircases of the figure 9. No gain variation is registered.

3.2 BGA CITIROC 1A evaluation board staircase measurements

We repeated the same staircase measurements by using the BGA CITIROC 1A evaluation board. This board, contrarily to the QFP board, has a 10KOhm in the HV circuit.

Operating the SiPMs in the same conditions as for the QFP board, we carried out the staircase measurements. Figure 11 shows the staircases obtained at different current flowing in the HV circuit produced by illuminating the 2x2 7x7 mm^2 with the continuous source.

The black line is the reference one. As can be noted we have a similar behavior of that of the QFP board but everything happens at currents 10 times lower. This behavior was expected because the 10 KOhm resistor in the HV circuit.

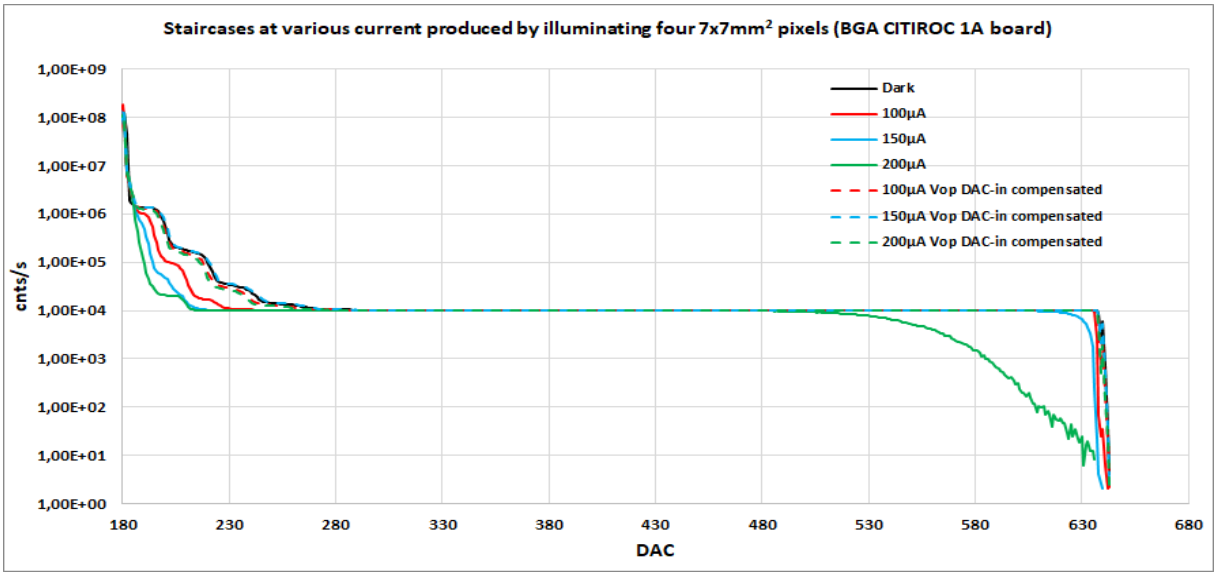


Figure 11. Staircases at different currents for the BGA CITIROC 1A evaluation board. As can be noted the current levels are ten times lower than the QFP board case. The dotted plots are those obtained by DAC input levels compensation.

Again, to better estimate the gain variation (solid lines) and the recovering (dotted lines), we reported in figure 8 the first part of the staircases.

As can be noted the dotted plots shows how the gain degradation is completely recovered by increasing the DAC input voltage level.

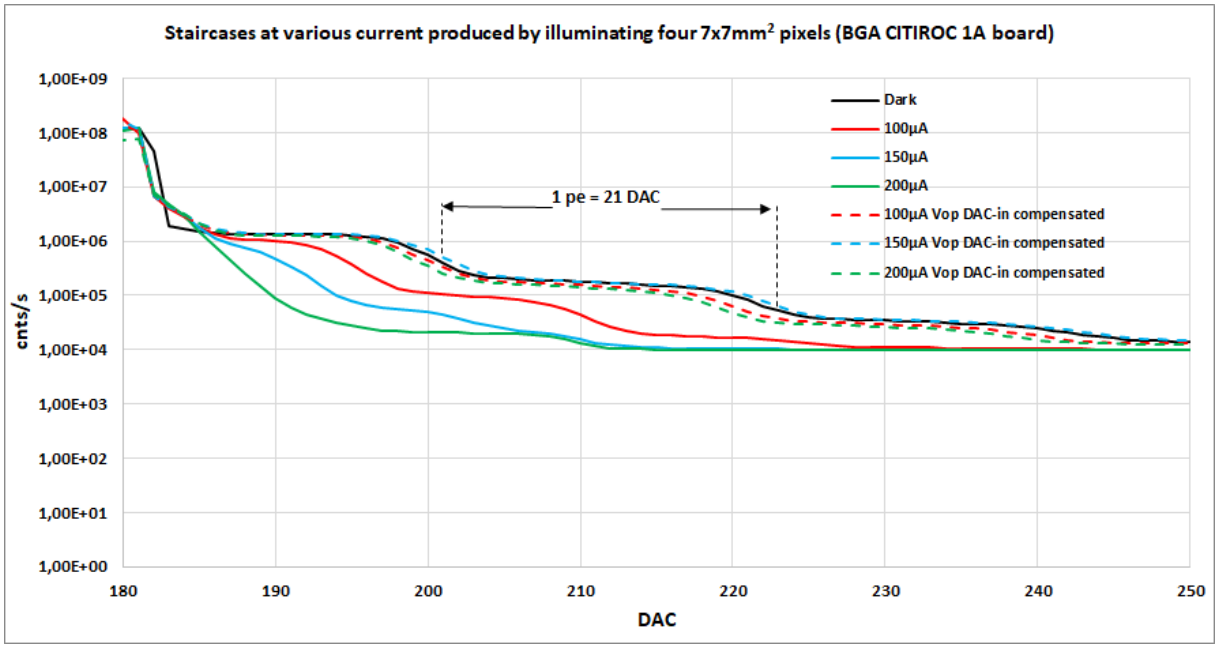
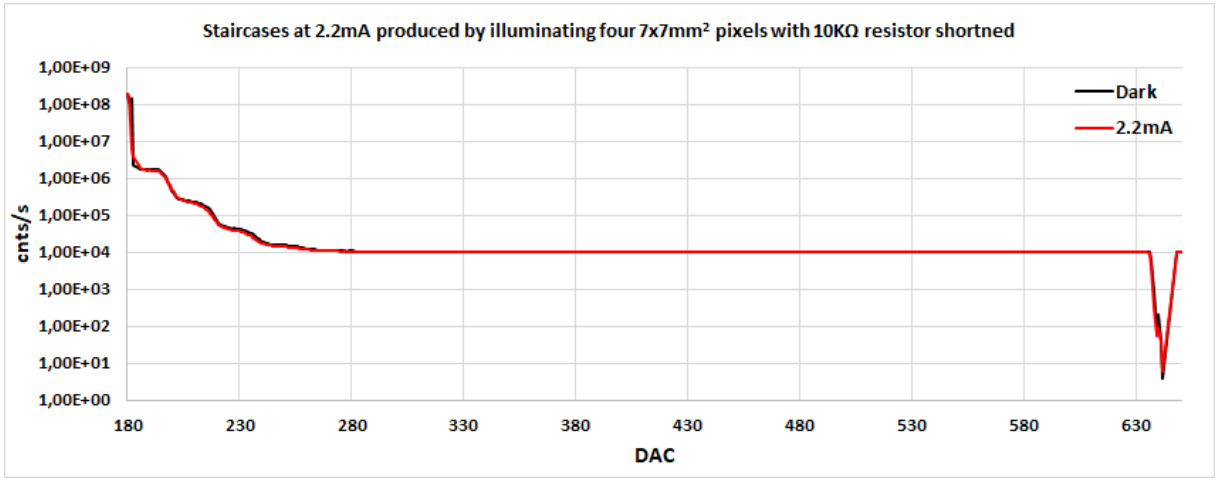


Figure 12. First part of the staircases of the figure 11. As can be noted the dotted plots shows how the gain degradation is completely recovered by increasing the DAC input voltage level.

As above mentioned, the effect of Vop decreasing is to be attributed to the 10KOhm resistor in the HV circuit. Then we shortened the resistor and repeated the staircase measurements.

Figure 13 shows the staircases obtained at 2.2 mA current flowing in the HV circuit. As can be noted no effect are present both in gain variation and drop in the final part of the plot.



4. Conclusions

The purpose of this work is to evaluate the influence of a relatively high continuous light flux on the SiPM gain. The staircase measurements demonstrated that the gain is only influenced if a resistor in the HV circuit is present. We have to care about also to each single 1Kohm resistor present in each channel in the HV filters. These could be responsible to lower the Vop voltage level and then the gain.

Thus we can conclude that the chip itself is not affected by high current flowing in the HV circuit even at current higher than 2.2 mA (more than 0.5mA per pixel). That in other words means that if the array is illuminated with a high level night sky background, the chip will maintain the same performance.

All files related to the experimental measurements presented in this report, are located in the database on the PC-LAB (COLD) site Astrophysical Observatory of Catania, path C:\Users\CCDLab1\Desktop\Romeo\Misure